Hardware co-simulation for a low complexity PAPR reduction scheme on an FPGA

ABSTRACT

This paper presents a novel low-complexity technique for reducing the Peak-to-Average Power Ratio PAPR in Orthogonal Frequency Division Multiplexing OFDM systems followed by an efficient hardware co-simulation implementation of this technique by using a Xilinx system generator on a Field Programmable Gate Array FPGA. In this technique, each subblock is interleaved with the others, and a new optimisation scheme is introduced in which the number of iterations is equal only to the number of subblocks, which results in reduced processing time and less computation that, in turn, leads to reduced complexity. Furthermore, the proposed method focuses on simplifying the required hardware resources. Thus, it can be easily combined with other simplified techniques. The simulation results demonstrate that the new technique can effectively reduce the complexity up to 98.22% compared with the new existing Partial Transmit Sequence PTS techniques and yield a good Bit Error Rate BER performance. Through the comparison of performance between simulation and hardware, it is distinctly illustrated that the designed hardware block diagram is as workable as the simulation and the difference of the result is only 0.1 dB.

Keyword: OFDM; Hardware co-simulation; FPGA; PAPR reduction; Peak-to-average power ratio; Orthogonal frequency division multiplexing; Field programmable gate arrays; Optimisation; Simulation; Partial transmit sequence; PTS; Bit error rate; BER